Coupled TCAD-SPICE Simulation of Parasitic BJT Effect on SOI CMOS SRAM SEU

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Abstract

Single event upsets (SEU) produced by heavy ions in SOI CMOS SRAM cells were simulated using a mixed-mode approach, that is, two-dimensional semiconductor device simulation by TCAD tool coupled with circuit SPICE simulator. The effects of parasitic BJT and particle strike position on the SOI CMOS SRAM cells upset for transistor length scaling from 0.25 µm to 65nm are presented.

1. Introduction

Single-event upset (SEU) of VLSI are very important for microelectronic equipment in space. The effect of the CMOS device scaling down and improvements in semiconductor device performance on circuit SEU were widely studied in the last years [1-3]. Work [3] presented some basic concepts and trends for single-event upset in highly scaled CMOS and SOI CMOS devices. As it was mentioned in the paper charge collection and SEU in SOI transistors are very complicated, and are heavily influenced by factors such as: the geometry of the structure and sizes of the areas, operating voltage, channel doping. SOI CMOS circuits from the one hand provide more SEU hardness in comparison with conventional (“volume”) circuits, but to the other hand parasitic BJT in SOI technology results to SEU pulses amplification and SEU resistance lowering [4]. Parasitic BJT effect on SRAM SEU depends on SOI CMOS structure features and distance of the strike location to the drain junction [5]. Using physics-based equations, the paper [5] showed how to break up each critical 0.15 µm SOI MOSFET transistor layout into several “boxes”, each with its own dimensions and critical charge, for the purpose of calculating soft error rate (SER). In order to achieve better performance of modern MOSFETs (65 nm and less) many design changes are incorporated: the use of special “halo” implants under the source and drain region, complex retrograde doping profiles in the channel region [3]. These doping features reduce the ion collected charge and enhance SEU hardness.

Unfortunately, the detailed analysis of parasitic BJT influence on SRAM SEU process for SOI MOSFET scaling was not presented enough.

The purpose of this work was to investigate the effects of the distance of the strike location to the drain, technology features, parasitic bipolar transistor action on SRAM cell SEU special aspects of for SOI MOSFETs scaled down to 65nm.

As soon as the single event transients (SETs) depend not only the MOSFET structure under the strike but also the whole SRAM cell circuit behavior, the most correct SEU simulation can be achieved by coupling the TCAD (structure) simulator with the SPICE (circuit) simulator [4]. Such combined approach provides more correct results in comparison with the only TCAD or SPICE simulations [4] and was used in the work.

2. Simulated SOI MOSFET structures

SOI MOSFET sizes were scaled down according to the known ITRS roadmap [6].

| Table 1. Parameters of the simulated SOI MOSFET structures |
|---------------------------------|-----|-----|-----|
| L_pr, um | 0.25 | 0.1 | 0.065 |
| t_gatox, nm | 5 | 3 | 1.7 |
| t_Siox, nm | 100 | 40 | 30 |
| t BOX, nm | 140 | 100 | 80 |
| W, um | 0.8 | 0.4 | 0.26 |
| V_supply, V | 2.5 | 1.2 | 1 |

Fig. 1 Scheme of coupled TCAD–SPICE simulation of SEU in CMOS SOI SRAM cell caused by heavy ion strike
The strikes of the ion with LET = 21 MeV·cm²/mg perpendicular to the surface of SOI MOSFET structure with a gate lengths of 0.25, 0.1 and 0.065 um (see Table 1) were modeled. The points of ion strikes are marked on the MOSFET layout in Fig. 2.

![MOSFET layout with the indication of ion strike points](image)

**Fig. 2 MOSFET layout with the indication of ion strike points**

### 3. SRAM cell SEU simulation results

Effects of ion strikes into the SOI n-MOSFET were analyzed at the different points after hitting as follows:
- analysis of the potential and the charge carriers distributions in n-MOSFET structure;
- detection of the parasitic n⁺-p⁻ BJT switching on/non-switching;
- calculation of the total charge collected at the drain;
- comparison of the collected charge with the deposited one;
- drain current pulse shape analysis;
- detection of the cell upset.

The modeling results are presented below.

Fig. 3 shows the electrostatic potential distribution in the 0.25 and 0.065 um n-MOSFET structures at the different time moments after ion strike.

Fig. 4 shows the drain current pulse shapes induced by ions hitting into the different points of the n-MOSFET layout.

Fig. 5 shows the values of the charge collected by drain at the points 5 of n-MOSFET with channel lengths of 0.25 um, 0.1 um and 0.065 um.

To estimate the current gain of the SOI MOSFET parasitic bipolar transistor the analogous SOI MOSFET structures (with different gate lengths) with grounded gate and 2 kOhm load resistor were simulated by TCAD tool using supply voltages of 2.5V for 0.25 um gate length, 1.2V for 0.1 um and 1V for 0.065 um. The current gain of parasitic bipolar transistor with a "floating" basis was calculated as in [7]: \( \beta = \frac{Q_{col}}{Q_{top}} \). The calculated values are shown in Fig. 5.

### 3.1 Ion strike into 0.25 um channel length SOI MOSFET structure

Ion strike into the source/drain regions (points 1, 2, 6, 7 (see Fig.2)). In this case the track is placed in highly doped n⁺ regions. There is no electric field in these regions, the electrons and holes can not be separated, and recombination process dominates. Only a small part of the minority carriers that reach the drain-substrate junction contributes the drain current. The charge collected by the drain has the maximum value (see Fig. 5(a)). The effect of the parasitic bipolar transistor is absent.

**Ion strike into the gate-drain area (point 5).** A few picoseconds after the ion strike the track eliminates the space-charge region (SCR) of the drain-substrate junction (see Fig. 3). Then the track electric field separates the generated electron-hole pairs and pushes electrons away to the drain and holes to the source through the channel region. The holes concentration in the channel area increases, which lowers the source-channel junction potential barrier and leads to the parasitic bipolar transistor opening and current amplification. It increases the charge collected at the drain (deposited charge - 21.6 fC, collected charge - 85.1 fC) (see Fig. 5(a)). Current pulse results to transistor M3 opening and memory cell upset. As a result transistor M1 becomes closed that stops transistor M2 drain current and ends current pulse.

**Ion strike into the gate center (points 4).** In this case the track is located in the middle of the working area. The parasitic bipolar transistor opens too, but the drain current increases for a longer time (see Fig. 3) than in the previous case. The cell upset also occurs.

**Ion strike into gate-source area (point 3).** The processes are similar to the previous case but they are slower. The collected charge has the largest value. As the amplitude of the current peak isn’t high enough the voltage drop at the drain of MOSFET M1 (see Fig.1) is not enough to open MOSFET M3 thus no upset happens.

**Ion strike into the drain region near the gate (point 9).** The simulation results show that ion is located nearly the reverse-biased drain pn-junction. Track charge is collected by junction internal electric field. The collected charge is enough for cell upset.

However, the farther track is located from the drain pn-junction the lesser charge is collected.

### 3.2 Ion strikes into 0.1 um channel length SOI MOSFET structure

**Ion strike into the electrically neutral source/drain junction regions (points 1, 2, 6 and 7).** Like in the case of 0.25 um gate length MOSFET, track carriers recombine and noticeable drain current pulse isn’t observed. There is no effect of parasitic bipolar transistor and no cell upset.
Ion strike into the gate region, gate-source, gate-drain, drain region nearly the junction (points 3, 4, 5, 9). Since SOI MOSFET with 0.1 um channel length is fully depleted, the track charge moves by drain junction electric field significantly faster (drift mechanism) than in 0.25 um transistor (diffusion mechanism). Therefore, the drain current pulses for these points are very similar, have a short duration and large amplitude and lead to cell upset. As the upset transient process is fast enough and transistor M1 is closed in time about 40 ps after ion strike and the transistor M2 switch off, then the drain collects only a portion of the deposited charge ($Q_{dep}=8.65$ fC, $Q_{col}=6-7$ fC).

In case of ion strike into source area nearly the gate (point 8) the parasitic bipolar transistor opens (similar to the point 3 of the 0.25 um length transistor). There is an additional electron current through active area to the drain that increases collected charge in comparison with the deposited one for 49% ($Q_{dep}=8.65$ fC, $Q_{col}=12.9$ fC). The process is extended in time, the magnitude of the drain current pulse is low, M2 drain voltage drop is not enough to open M3 and cell upset does not occur.

### 3.3 Ion strike into 0.065 um channel length SOI MOSFET structure

The simulation results were similar to the results for the 0.1 um channel length SOI MOSFET. The main difference is the lower value of the collected charge (no more than 7 fC) and the deposited charge ($Q_{dep}=5.61$ fC). This fact is under consideration [3], but the main reason for this behavior is the very small size of areas in modern MOSFETs.

### 3.4 Effect of doping level on SEU

As it was mentioned the modern MOSFETs (65 nm and less) incorporate many design changes in order to achieve better performance [3]. Halo doping was used in the considered 0.065 um SOI n-MOSFET. To estimate the effects of these technology features transistor structure with a lower working area doping (two times lower) was simulated. The simulation results showed that in all points the collected charge has increased by nearly 3 times. But there were not new SEU observed in considered points. However new SEUs have appeared in the point located between points 8 and 3.

The effect of the parasitic BJT on SEU, simulated collected charge (left) and parasitic BJT current gain BAF (right) for the n-MOSFET with channel lengths of 0.25 um, 0.1 um and 0.065 um are presented in Fig. 5.
4. Conclusion

Coupled TCAD-SPICE simulation results of SOI n-MOSFET structure and in SRAM cell circuit under the ion strike for gate lengths of 0.25, 0.1 and 0.065 um with account for the strike location positions were performed.

The detailed analysis of the simulated electrostatic potential and charge carriers distribution in the SOI MOSFET structure showed that the upset process in the cell is strongly influenced by the three factors:

1) The current gain of the parasitic n’-p-n’ bipolar transistor with the floating base;
2) The amplitude and slope of the drain current pulse induced by ion strikes;
3) Ion strike position on SOI MOSFET layout.

The first two factors effect equally: with their increase the probability of cell failure increases.

The third factor influences differently:

- for 0.065 um and 0.1 um MOSFET devices ion strike into the gate area and the drain and source pn-junction areas results to cell upset;
- for 0.25 um device ion strike into the gate and the drain pn-junction areas results to upset, while ion strike into the source pn-junction area doesn’t.

It was shown that the probability of the cell failure increased with MOSFETs gate length scaling down. However, SOI MOSFET transistors with 0.1 um and 0.065 um gate sizes showed identical sensitivity to ion strike. That may be explained by a smaller transistor area and more doping level for 0.065 um transistor.

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5. References


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