National Research University High School of Economics

as a manuscript

Ismail-Zade Mamed Rashidovich

Development and research of MOSFET and JFET compact SPICE models with account for thermal effects

Dissertation summary
for the purpose of obtaining academic degree
Doctor of Philosophy in Engineering

Academic supervisor:
Doctor of Technical Sciences,
Professor
Petrosyants Konstantin Orestovich

Moscow – 2021

Relevance of the research topic

The specificity of the development and design of electronic equipment for the space industry, nuclear power, satellite and telecommunication systems, the aerospace industry and other special applications is the need to take into account the thermal effects caused by the influence of external high or low temperatures, as well as internal self-heating due to the power dissipated in electronic components.

The reliability of the electronic components of the listed devices is subject to increased requirements, which are provided by: new design and technological, circuit and system engineering solutions; special materials, structures and protective equipment; more "harsh" methods of designing devices and circuits exposed to temperature. The effectiveness of using these approaches is necessarily confirmed by the results of field tests. It should be noted that testing and experimental work is carried out using complex, sometimes unique measuring equipment and experimental techniques that require large time and material costs. In some cases, obtaining experimental information is difficult or impossible.

Under these conditions, the role of mathematical modeling methods increases significantly, allowing in most cases to give a reliable forecast of changes in the electrical characteristics of devices and circuits exposed to temperature and to give predictive estimates of its durability and reliability. At the same time, as a rule, it is possible to minimize the volume of necessary tests and measurements to a reasonable minimum and significantly reduce time and logistical costs.

The main market share of modern ICs and LSIs includes circuits based on silicon MOSFETs and JFETs. For their development and design, commercial CAD systems are widely used, including tools for process&device and circuit modeling. However, their use as applied to the devices and circuits operating under conditions of exposure to ultra-high (up to +300°C) and ultra-low (down to –200°C) temperatures is ineffective. The reason is that in commercial CAD systems the range of applicability of the built-in SPICE-models of MOSFETs and JFETs of various types is limited to the standard range of –60°C…+125°C.

In addition to the development of the MOSFET and JFET SPICE models, the problem of determining their parameters for an extended temperature range arises. In the available publications, this issue is extremely insufficiently covered.

Thus, this work aims to remove the existing limitations in terms of accounting for thermal effects in SPICE models of MOSFET and JFET transistors manufactured using existing and promising silicon technologies.

The purpose and objectives of the research

The purpose of the thesis is the development and research of MOSFET and JFET SPICE-models for simulating electronic circuits operating in an ultra-wide temperature range (–200°C…+300°C).

To achieve this goal, the following **tasks** were solved:

1) New and improved existing compact SPICE models of MOSFET and JFET-transistors taking into account thermal effects by including additional expressions for temperature-dependent parameters in the model have been developed;

2) Procedures for determining the parameters of MOSFET and JFET SPICE models based on the results of measuring their electrical, capacitive and thermal characteristics in the wide temperature range have been developed;

3) Software for controlling an automated hardware-software complex that implements procedures for measuring electrical characteristics and extracting parameters of SPICE-THERM models has been developed;

4) The developed libraries of SPICE-models are built into schematic CAD systems, which made it possible to significantly expand the possibilities of their application in the field of assessing the resistance to temperature of ICs and LSIs;

5) The developed models and methods for determining their parameters are used for the design of various structural and technological varieties of temperature-resistant ICs and LSIs built on MOSFET and JFET transistors.

Research methods

To solve the problems posed in the thesis, methods of experimental determination of the electrical characteristics of test structures, mathematical methods of processing measurement results, methods of approximation and optimization, computer analysis and modeling, methods of conducting computational experiments were used.

The degree of elaboration of the research topic

The problem of modeling JFET transistors in the temperature range is extremely insufficiently studied. There are practically no works on modeling static *I–V* characteristics.

Among the few works, can be noted the works of domestic authors Dvornikov O.V., Prokopenko N.N. and Pilipenko A.M., and among foreign ones Y. Wang, Kostopoulos K., C. Patil, dedicated to low- and high-temperature versions of SPICE-models of JFET transistors for the problems of analyzing noise characteristics in small-signal mode of temperature-resistant analog ICs.

The development and research of MOSFETs compact SPICE-models, taking into account the influence of low (down to –200°C) and high (up to +300°C) temperatures, reflected in the works of the authors Petrosyants K.O., Pilipenko A.M., Kharitonov I.A., Jeon D.S. & Burk D.E., Cheng Y., Akturk A., Zhao H. and others.

In these, works two approaches to the formation of a compact SPICE model are worth noting: 1) including an additional subcircuit to the standard model, which takes into account the influence of the low/high temperature range; 2) using a set of software functions in the Verilog-A language, which is then connected to the standard MOSFET model.

The analysis of existing works showed that 1) some models cover a limited temperature range; 2) there is practically no unified model that takes into account a wide range of cryogenic and ultra-high temperatures; 3) the methods of extracting the parameters of Low-T and High-T SPICE-models have not been worked out to

the proper extent; 4) there are no high-temperature versions of the SPICE model for promising field devices with the UTBB FDSOI MOSFET and FinFET structures with deep submicron and nanometer sizes.

The author's personal contribution to the research

The author's personal contribution to the dissertation work is as follows:

1) Literature review and a theoretical analysis of the problem has been completed.

2) Low- and high-temperature versions of compact SPICE models for traditional submicron MOSFETs and promising nanoscale MOSFETs with FinFET structure on bulk silicon and on an insulating substrates have been developed.

3) Low- and high-temperature versions of compact SPICE models for JFET transistors have been developed.

4) For all the developed models, verification was carried out on specific examples that allow us to give predictive estimates of resistance to temperature.

5) Electrical characteristics were measured in the temperature range from room temperature to + 300°C for a 0.18-μm SOI CMOS structure fabricated by Mikron Group and for a 0.5-μm SOI CMOS structure fabricated by SRISA, as well as processing and analysis of the obtained experimental measurement results.

6) Participation in the development of an automated hardware and software complex for measuring the electrical characteristics of integrated MOS transistors and extracting the SPICE models temperature parameters.

7) The analysis of the obtained results was carried out, conclusions on the dissertation work were formulated.

Scientific novelty of research

1) A compact SPICE-THERM model has been developed for silicon-based JFETs, which is valid in an ultra-wide temperature range from –200°C to +300°C; for silicon carbide-based JFET (SiC), the upper limit of the SPICE model has been extended to +500°C. The description of the standard JFET Level 3 model was augmented with new semi-empirical temperature dependences for saturation

voltage, pinch off current, transconductance, threshold voltage, drain/source resistances and other parameters.

2) For integrated MOS transistors manufactured using various submicron and promising nanometer technologies, versions of SPICE-THERM models have been developed that are valid in an ultra-wide temperature range (-200°C…+300°C), including:

- For submicron and deep submicron SOI MOSFETs, low-temperature (down to –250°C) and high-temperature (up to +300°C) versions of the SPICE model based on BSIMSOI v4 are developed. Compared to existing SPICE models, the proposed low-temperature SPICE model additionally takes into account the temperature-induced shift of the subthreshold slope, which is important for low-voltage and low-power devices. For the high-temperature SPICE model, new temperature dependences are introduced for the threshold voltage shift and temperature-induced leakage currents.
- A low-temperature version (down to –269°C) of the BSIM4 SPICE model has been developed for 0.25-μm silicon on sapphire (SOS) MOSFETs. The model takes into account the influence of the kink effect, with the help of an additional voltage-controlled voltage source serially connected to the gate contact. A procedure for determining the model parameters has been developed.
- Low-temperature versions of PSPv103.1 and BSIM6 SPICE-models have been developed for 28-nm Bulk MOSFETs. New semi-empirical temperature dependences for the carrier mobility, threshold voltage, saturation rate, impact ionization current, and Coulomb scattering are introduced into the description of the models.
- For 28-nm MOSFETs fabricated on silicon-on-insulator (SOI) structures, a version of the UTISOIv.2 model has been developed, which is valid in an ultra-wide temperature range (–200°C…+300°C). In the description of the model, corrective functions for the dependence on temperature for the threshold voltage, mobility, subthreshold slope and others are introduced.

- For sub-100 nm FinFET-transistors with a triple gate on bulk silicon and an insulating substrate, low-temperature (down to –265°C) and high-temperature (up to +250°C) versions of BSIM-CMG v107 SPICE-model have been developed.

Provisions presented for defense

1) A set of low- and high-temperature versions of SPICE-models for various design and technological varieties of MOSFETs, manufactured according to traditional submicron and advanced sub-100 nm CMOS technological processes:

- High-temperature versions of the SPICE model: 0.18-μm and 0.5-μm SOI MOSFETs, sub-100 nm FinFET and UTBB FDSOI MOS transistors;
- Low-temperature versions of the SPICE model: 0.18-μm SOI MOSFET; 0.25-μm and 0.5-μm SOS MOSFETs; 28-nm UTBB FDSOI MOSFET, 28-nm Bulk MOSFET; sub-100 nm FinFET transistors;

2) Compact SPICE-THERM model of JFET-transistor, valid in the ultra-wide temperature range from –200°C to +300°C; an automated procedure for determining the SPICE-THERM model parameters of JFET based on the results of measurements of a standard *I–V* characteristics set in the wide temperature range.

3) Additional software module for automated calculation of SPICE-models temperature parameters of transistor structures based on the results of electrical characteristics measurements;

4) The results of using the temperature versions of the MOSFET and JFET SPICE-models in the practice of designing various constructive and technological varieties of temperature-resistant circuits.

The practical significance

1) The developed SPICE-THERM models are embedded in the libraries models of industrial CADs: ADS (Keysight Technologies), HSpice (Synopsys), LTSpice (Analog Devices), Multisim (National Instruments) and can be used to design of various structural and technological varieties of resistance to temperature ICs and LSIs based on MOSFET and JFET transistors.

2) For users of the universal extractor of parameters of electronic components IC-CAP, an additional software modules have been developed for automated calculation of the temperature parameters of SPICE-models of transistor structures based on the results of measurements of electrical characteristics. Two certificates of registration of a computer program were received (RU 2019614991 and RU 2017663307).

The degree of reliability of the obtained results

The reliability of the results obtained in the dissertation research is confirmed by:

1) The coincidence of the simulation results with the experimental electrical characteristics of all types of MOSFET and JFET structures considered in the thesis, in the studied temperature ranges, which is sufficient for practical calculations.

2) The data of similar published works of domestic and foreign experts, confirming the results obtained in the dissertation.

Using the results of work

The results of the dissertation were used when performing work at the following enterprises and organizations:

1) Federal State Budgetary Scientific Institution "Research Institute of Advanced Materials and Technologies" within the framework of R&D "Research of advanced circuits of extreme electronics in an extended temperature range (-200…+300°C)". 2017-2019.

2) JSC Zelenograd Innovation and Technology Center within the framework of research and development "Research and development of technologies for the component base of high-temperature micro- and nanoelectronics", 2017.

3) Institute of Microelectronics of the China Academy of Sciences, Beijing, within the framework of the RFBR joint project "Experimental and theoretical research and modeling of nanoscale semiconductor devices taking into account the influence of various radiation factors", 2020

4) JSC "Minsk Research Institute of Instrument Engineering" in the framework of joint work on the use of analog BMK elements for the construction of sensor systems.

And also when performing work on grants from the Russian Foundation for Basic Research (2014, 2018, 2020) and the Scientific Fund of the National Research University Higher School of Economics (2018, 2019).

General conclusions of the research

In the dissertation work, an important task was solved – a significant expansion of the field of applicability of SPICE-models of field-effect transistors used in industrial CADs. The existing standard temperature range of -60°C…+125°C has been extended to ultra-low (–270°C) and ultra-high (+300°C) temperatures. This predetermines its relevance and practical significance, since the market share for electronic components operating in extreme conditions is steadily expanding, and, according to experts, this trend will only intensify.

The applicant has carried out a large amount of research and obtained significant results in both theoretical and experimental fields.

In the field of theory:

• Low- and High-temperature modifications of SPICE models of MOSFET, FinFET and JFET transistors on bulk and silicon on insulator (SOI) and silicon on sapphire (SOS) structures have been developed. In comparison with the previously existing SPICE models, the temperature effects of the subthreshold voltage shift, changes of the mobility, the occurrence of leakage currents, the kink effect, etc. are additionally taken into account.

• The procedure for determining the SPICE-THERM model parameters from the results of measuring the I–V characteristics of transistors in the high and low temperatures range have been developed.

In the practical area:

• The measuring procedures and software for processing the results of measuring the I–V characteristics of devices in the temperature range have been modified. Two certificates for registration of computer programs were obtained.

• A large amount of measurements of the characteristics of MOSFET transistors was carried out in the wide temperatures range used in domestic enterprises; the procedure for extracting their SPICE parameters was carried out and databases were formed for circuit design of CMOS ICs and LSIs operating in an extended temperature range. The effectiveness of the use of the results is confirmed by the Research Institute of Advanced Materials and Technologies (RIAMT) and the Zelenograd Nanotechnological Center.

• The developed MOSFET SPICE-THERM models are embedded in the libraries models of industrial CADs: LTSpice (Analog Devices), Multisim (National Instruments), ADS (Keysight Technologies), HSpice (Synopsys). In total, 6 THERM versions have been developed for various types of SPICE models; 10 constructive and technological varieties of MOSFETs from various manufacturers. This predetermines a wide range of specialist users of the results obtained in the dissertation.

Work approbation

The main results of the work were reported and discussed at the following scientific events:

1) Science and Technology Conference for Students, Postgraduates and Young Professionals of the Higher School of Economics named after E.V. Armensky.– M.: MIEM NRU HSE, 2015 - 2017;

2) International Forum "Microelectronics-2016, 2018, 2019, 2020". 2nd, 4th, 5th and 6th International Scientific Conference "Electronic Component Base and Microelectronic Modules". Republic of Crimea, Alushta, 2016, 2018, 2019, 2020;

3) International Workshop on Reliability of Micro- and Nano-Electronic Devices in Harsh Environment (IWRMN-EDHE 2017). Chengdu, China, 2017;

4) XVI, XVII All-Russian Scientific and Technical Conference "Electronics, Micro- and Nanoelectronics". Suzdal, Russia. 2017, 2018;

5) XVI, XVII, XVIII Scientific and practical seminar "Problems of creating specialized radiation-resistant VLSIs based on heterostructures." - N. Novgorod, 2016 - 2018;

6) XVIII, IX All-Russian scientific and technical conference "Problems of the development of promising micro- and nanoelectronic systems (MES)". - Moscow, 2018, 2020;

7) IEEE East-West Design & Test Symposium (EWDTS). 2017, 2018;

8) IEEE Conference of Young Researchers in Electrical and Electronic Engineering (ElConRus). - Moscow-Zelenograd, 2017;

9) 2018, 2020 Moscow Workshop on Electronic and Networking Technologies (MWENT). - Moscow, 2018, 2020.

List of published articles that contain key thesis results

The main provisions of the scientific research are presented in 28 works (from 2015 to 2021 years), of which 10 in edition indexed in the Web of Science and Scopus databases, 3 in edition included in the list of recommended journals of the Higher School of Economics, 3 works published without co-authors.

Publications in journals indexed in the Web of Science and Scopus databases:

1. Petrosyants K.O, Sambursky L.M, Kozhukhov M.V, **Ismail-zade M.R**, Kharitonov I.A, Li Bo. SPICE Compact BJT, MOSFET and JFET Models for ICs Simulation in the Wide Temperature Range (from –200 ° C to + 300 ° C) // IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 2021. Vol. 40. No. 4. P. 708-722. (quartile Q2).

2. Petrosyants K.O, **Ismail-zade M.R.**, Sambursky L.M. Compact Si JFET Model for Cryogenic Temperature // Cryogenics. 2020. Vol. 108. P. 1-6. (quartile Q2).

3. K.O. Petrosyants, **M.R. Ismail-Zade**, L.M. Sambursky. The Special Features of Simulation of the Current – Voltage Characteristics of JFETs in the Cryogenic Temperature Range // Russian Microelectronics. 2020. Vol. 49. No. 7.P. 501-506. (quartile Q3).

4. Lev M. Sambursky, **Mamed R. Ismail-zade**, Nina V. Blokhina. Early Study of Transistor and Circuit Parameter Variation for 180 nm High-Temperature SOI CMOS Production Technology, in: 2020 Moscow Workshop on Electronic and Networking Technologies (MWENT). IEEE, 2020. P. 1-7.

5. Petrosyants K.O., **Ismail-zade M.R.**, Sambursky L.M., Dvornikov O.V., Lvov B.G., Kharitonov I.A. Automation of Parameter Extraction Procedure for Si JFET SPICE Model in the −200 ... +110°C Temperature Range, in: 2018 Moscow Workshop on Electronic and Networking Technologies (MWENT). Proceedings. M.: IEEE, 2018. P. 1-5.

6. Lev M. Sambursky, Dmitry A. Parfenov, **Mamed R. Ismail-zade**, Alexander S. Boldov, Borislav S. Dubyaga. Prediction of High-Temperature Operation (up to + 300 ° C) of Reference Voltage Source Built with Temperature-Tolerant Production Technology, in: Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2018). IEEE Computer Society, 2018. P. 609-613.

7. Petrosyants K.O., Sambursky L.M., Kharitonov I.A., **Ismail-zade M.R.** Generalized Test Automation Method for MOSFET's Including Characteristics Measurements and Model Parameters Extraction for Aero-Space Applications, in: Proceedings of XV IEEE East-West Design & Test Symposium (EWDTS'2017) ... Piscataway: IEEE, 2017. P. 504-511.

8. **Mamed R. Ismail-zade**, Aleksandr Y. Romanov, Egor Y. Kuzin, Vladimir S. Danykin, Igor A. Chetverikov. Hardware-Software System for Automation of Characteristics Measurement of SOI CMOS VLSI Elements under Extreme High Temperature Conditions (up to 300 ° C), in: Proceedings of the 2017 IEEE Russia Section Young Researchers in Electrical and Electronic Engineering Conference (2017 ElConRus) Part 2 . M.: IEEE, 2017. P. 423-428.

9. Petrosyants K.O., Lebedev S.V., Sambursky L.M., Stakhin V.G., Kharitonov I.A., **Ismail-zade M.R.**, Ignatov P.V. High temperature submicron SOI CMOS technology characterization for analog and digital applications up to 300 ° C, in: 33rd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM). PROCEEDINGS 2017. Denver: IEEE, 2017. P. 229-234.

10. Petrosyants K.O., Kharitonov I.A., Sambursky L.M., **Ismail-zade M.R.** Complex for automated measurement and processing of BJTs and MOSFETs characteristics for extremal applications, in: 2016 International Siberian Conference on Control and Communications (SIBCON). Proceedings. M.: HSE, 2016. P. 1-4.

Publications in journals included in the HSE's list of recommended journals:

11. **Ismail-Zade M.R.** JFET and MOSFET SPICE models in wide temperature range. Proc. Univ. Electronics, 2020, vol. 25, no. 1, pp. 40–47.

12. Petrosyants K.O., **Ismail-Zade M.R.**, Samburskiy L.M., Kharitonov I.A., Silkin D.S. SPICE-models for taking into account radiation and low-temperature effects in sub-100 nm MOS-transistor structures / / Nanoindustry. 2020. T. 13. No. S5-2. S. 386-392.

13. Petrosyants K.O., **Ismail-Zade M.R.**, Sambursky L.M. Highlights of JFET I-V characteristics simulation in cryogenic temperature range. Proc. Univ. Electronics, 2019, vol. 24, no. 2, pp. 174–184.

Publications in other editions:

14. **Ismail-Zade M. R.**, Samburskiy L. M. SPICE models of submicron CMOS transistors in the cryogenic temperature range // In the book: International Forum "Microelectronics-2020". School of Young Scientists. Collection of abstracts. Republic of Crimea, Yalta, September 21-25, 2020 M.: MAKS Press, 2020.S. 229-232.

15. Petrosyants KO, Popov DA, **Ismail-zade MR**, Sambursky LM, Bo Li, Wang YC TCAD and SPICE Models for Account of Radiation Effects in Nanoscale MOSFET Structures // Problems of Perspective Micro- and Nanoelectronic Systems Development - 2020. Issue 4. P . 2-8.

16. **Ismail-Zade M. R.** SPICE-models JFET and MOSFET in a wide temperature range (–200 ... + 300 ° C) // In the book: International Forum "Microelectronics-2019". School of Young Scientists. Collection of abstracts. Republic of Crimea, September 23-25, 2019 M.: Spectr LLC, 2019.S. 284-292.

17. Petrosyants K.O., **Ismail-zade M.R.**, Samburskiy L.M., Kharitonov I.A. SPICE-models of field-effect transistors with MOSFET and JFET structure for an extended temperature range up to –200 ° C // Problems of the development of promising micro- and nanoelectronic systems. 2018. Issue 3.P. 111-117.

18. Petrosyants K. O., Kharitonov I. A., Sambursky L. M., **Ismail-Zade M. R.** Principles of developing SPICE-model libraries of electronic components for critical applications of domestic production // In: International Forum "Microelectronics-2018". Collection of abstracts. Republic of Crimea, Alushta, 01-06 October 2018, Moscow: Technosphere, 2018. pp. 308-312.

19. Petrosyants K.O., Popov D.A., Samburskiy L.M., **Ismail-Zade M.R.**, Kharitonov I.A. // In the book: XVII All-Russian Scientific and Technical Conference "Electronics, Micro- and Nanoelectronics": May 14 - 18, 2018, Suzdal, Russia. M.: NIISI RAN, 2018.S. 67-68.

20. Petrosyants KO, Kharitonov IA, Kozhukhov MV, Sambursky LM, **Ismail-zade M.R.** An Efficient Approach to Simulation of Radiation Effects in bipolar and MOSFET IC's using Non-Specialized SPICE Simulators, in: 2017 International Workshop on Reliability of Micro- and Nano-Electronic Devices in Harsh Environment ”(IWRMN-EDHE 2017). Institute of Microelectronics of Chinese Academy of Sciences, 2017. P. 1-3.

21. Samburskiy L. M., **Ismail-Zade M. R.**, Kuzin E. Yu., Chetverikov I. A., Danykin V. S. Research of characteristics and determination of parameters of SPICE-models of submicron SOI MOSFET in the temperature range up to 300 ° C / In the book: XVI All-Russian Scientific and Technical Conference "Electronics, Micro- and Nanoelectronics": July 3 - 7, 2017, Suzdal, Russia. M.: NIISI RAN, 2017.S. 55-56.

22. Kharitonov I.A., Chetverikov I.A., Kuzin E. Yu., **Ismail-Zade M.R.** Determination of the parameters of SPICE-models of MOSFETs at low temperatures (up to minus 200 ° C) // Proceedings of NIISI RAN. 2017.Vol. 7.No. 2.P. 41-45.

23. Kharitonov I.A., Chetverikov I.A., Kuzin E.Yu**., Ismail-Zade M.R.** - technical conference "Electronics, micro- and nanoelectronics": July 3 - 7, 2017, Suzdal, Russia. M.: NIISI RAN, 2017.S. 66-67.

24. **Ismail-Zade M.R.** E.V. Armensky. Collection of abstracts. M.: MIEM NRU HSE, 2017.S. 282-283.

25. Petrosyants K.O., Kharitonov I.A., Samburskiy L.M., **Ismail-Zade M.R.**, Stakhin V.G., Lebedev S.V. Characterization of high-temperature CMOS IC elements // In the book: Problems of creation specialized radiation-resistant VLSI based on heterostructures. XVII scientific and practical seminar with international participation: collection of works. N. Novgorod: Federal State Unitary Enterprise “Federal Scientific and Practical Center NIIIS named after Yu.E. Sedakova ", 2017. S. 76-79.

26. **Ismail-Zade M.R.**, Samburskiy L.M. E.V. Armensky Conference materials. M.: MIEM NRU HSE, 2016.S. 280-281.

27. Lebedev S.V., Petrosyants K.O., Samburskiy L.M., Stakhin V.G., Kharitonov I.A., **Ismail-Zade M.R.** In the book: International Forum "Microelectronics-2016". 2nd Scientific Conference "Integrated Circuits and Microelectronic Modules". M.: Technosphere, 2016.pp. 237-238.

28. **Ismail-Zade M.R.**, Samburskiy L.M. Hardware and software complex for extracting the parameters of SPICE-models of MOS transistors taking into account the effect of stationary radiation // In the book: Scientific and technical conference of students, graduate students and young specialists of the Higher School of Economics them. E.V. Armensky. Conference materials. M: MIEM NRU HSE, 2015.S. 262-263.

Intellectual property objects:

1. Samburskiy L.M., **Ismail-Zade M.R.**, Petrosyants K.O., Kharitonov I.A. A program for determining the parameters of models of bipolar transistors, taking into account the temperature effect, based on the results of measurements of their electrical characteristics. Certificate of registration of the computer program RU 2019614991, 04.16.2019. Application No. 2019613506 dated 03.22.2019.

2. Samburskiy L.M., **Ismail-zade M.R.**, Chetverikov I.A., Petrosyants K.O., Kharitonov I.A. Program to determine basic parameters of submicron MOS - tranzistorov based on the results of measurement of their electrical characteristics " MOSPEDIUM ". Certificate of registration of the computer program RU 2017663307, 28.11.2017. Application No. 2017610866 dated 02.02.2017.