Syllabus

«Computer Architecture»

Approved by

The Academic Council

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Author	Nadezhda Trubochkina, Prof Dr
Credits	2
Contact work (hours)	10
Individual work (hours)	66
Course	1
The format of the discipline	Blended learning

I. Purpose, Learning Outcomes and Prerequisites

Purpose

Objectives of mastering the discipline "Computer Architecture":

- give students an idea of the principles of computer architecture;
- inculcate in students the skills of research work, which implies an independent study of the working documentation, specific tools and software tools that allow simulating the operation of a computer.

Learning Input

The study of this discipline is based on the following disciplines:

- Fundamentals of building software and hardware for computing systems
- Information systems and technologies

To master the discipline, students must possess the following knowledge and competencies:

- PC knowledge at advanced user level,
- understand of the principles of organization and functioning of the main computer units and the Armed Forces,
- knowledge of various number systems,

 knowledge of the principles of data storage and various types in the computer's memory.

Learning Outcomes

On completion of the course, the student should:

- understand the evolution of the distributed computing from its early beginnings as multi-processor and multi-computer systems, to computer networks, to the emerging cloud, edge (fog, dew) and heterogeneous computing environments;
- understand the existing distributed computing paradigms and systematic issues;
- understand application areas of distributed computing technology, such as scientific computing, big data, machine learning, data mining and virtual worlds;
- be familiar with existing computing techniques, technologies and tools;
- have built a distributed computing application system using available technologies and/or tools; understand evaluation techniques for successful design and development of efficient and effective application systems.

Prerequisites

- Fundamentals of building software and hardware computing systems and networks
- Information Systems and Technologies

Post requisites

- Design of corporate information systems
- Information security management systems
- Methodology and technology for developing corporate student expert systems
- Equipment of computer networks and telecommunication systems
- Simulation of computer networks and telecommunication systems
- Design and management of computer networks
- Designing wireless networks and mobile systems
- Architecture and integration of corporate information systems
- Master's dissertation

II. Topic-wise Course Content

Topic 1. Introduction, Instruction Set Architecture, and Microcode.

This lecture will give you a broad overview of the course, as well as the description of architecture, micro-architecture and instruction set architectures.

Course Introduction. Course Overview. Motivation. Course Content. Architecture and Microarchitecture. Machine Models. ISA Characteristics. Recap.

Topic 2. Pipelining Review.

This lecture covers the basic concept of pipeline and two different types of hazards.

Microcoded Microarchitecture. Pipeline Basics. Structural Hazard. Data Hazards.

Topic 3. Cache Review

This lecture covers control hazards and the motivation for caches.

Control Hazards, Jumps. Control Hazards, Branch. Control Hazards, Others. Memory Technologies. Motivation for Caches.

Topic 4. Superscalar 1

This lecture covers cache characteristics and basic superscalar architecture.

Classifying Caches. Cache Performance. Superscalar. Basic Two-way In-order Superscalar.Fetch Logic and Alignment.

Topic 5. Superscalar 2 & Exceptions

This lecture covers the common issues for superscalar architecture.

Baseline Superscalar and Alignment. Interrupts and Bypassing. Interrupts and Exceptions. Introduction to Out-of-Order Processors.

Topic 6. Superscalar 3

This lecture covers different kinds of architectures for out-of-order processors.

Review of Out-of-Order Processors. I2O2 Processors. I2O1 Processors. IO3 Processors. IO2I Processors.

Topic 7. Superscalar 4

This lecture covers the common methods used to improve the performance of out-of-order processors including register renaming and memory disambiguation.Speculation and Branch. Register Renaming Introduction. Register Renaming with Pointers to IQ and ROB. Register Renaming with Values in IQ and ROB. Memory Disambiguation.

Topic 8. VLIW 1

This lecture covers the basic concept of very long instruction word (VLIW) processors. Limits of Out-of-Order Design Complexity. Introduction to VLIW. VLIW Compiler. Optimizations. Classic VLIW Challenges. Introduction to Predication.

Topic 9. VLIW2

This lecture covers the common methods used to improve VLIW performance.

Scheduling Model Review. Review of Predication. Predication Implementation. Speculation Execution. Dynamic Events and Clustered VLIWs. Case Study: IA-64/Itanium.

Topic 10. Branch Prediction

This lecture covers the motivation and implementation of branch predictors.

Branch Cost Motivation. Branch Prediction Introduction. Static Outcome Prediction. Dynamic Outcome Prediction. Target Address Prediction.

Topic 11. Advanced Caches 1

This lecture covers the advanced mechanisms used to improve cache performance.

Basic Cache Optimizations. Cache Pipelining. Write Buffers. Multilevel Caches. Victim Caches. Prefetching.

Topic 12. Advanced Caches 2

This lecture covers more advanced mechanisms used to improve cache performance.

Multiporting and Banking. Software Memory Optimizations. Non-blocking Caches. Critical Word First and Early Restart.

Topic 13. Memory Protection

This lecture covers memory management and protection.

Memory Management Introduction. Base and Bound Registers. Page Based Memory Systems. Translation and Protection. TLB Processing.

Topic 14. Vector Processors and GPUs

This lecture covers the vector processor and optimizations for vector processors.

Address Translation Review. Cache and Memory Protection Interaction. Vector Processor Introduction. Vector Parallelism. Vector Hardware Optimizations. Vector Software and Compiler Optimizations.

Topic 15. Multithreading

This lecture covers different types of multithreading.

Reduction, Scatter/Gather, and the Cray. SIMD. GPUs. Multithreading Motivation. Coarse-Grain Multithreading. Simultaneous Multithreading.

Topic 16. Parallel Programming 1

This lecture covers the concepts of parallelism, consistency models, and basic parallel programming techniques.

SMT Implementation. Introduction to Parallelism. Sequential Consistency. Introduction to Locks.

Topic 17. Parallel Programming 2

This lecture covers the solutions for the consistency problem in parallel programming.

Sequential Consistency Review. Locks and Semaphores. Atomic Operations. Memory Fences. Dekker's Algorithm.

Topic 18. Small Multiprocessors

This lecture covers the implementation of small multiprocessors.

Locking Review. Bus Implementation. Cache Coherence. Bus-Based Multiprocessors. Cache Coherence Protocols.

Topic 19. Multiprocessor Interconnect 1

This lecture covers the design of interconnects for a multiprocessor.

More Cache Coherence Protocols. Introduction to Interconnection Networks. Message Passing. Interconnect Design.

Topic 20. Multiprocessor Interconnect 2

This lecture covers the design of interconnects for multiprocessor and network topology.

Networking Review. Topology. Topology Parameters. Network Performance. Routing and Flow Control.

Topic 21. Large Multiprocessors (Directory Protocols)

This lecture covers the motivation and implementation of directory protocol used for coherence on large multiproccesors.

Credit Based Flow Control. Deadlock. False Sharing. Introduction to Directory Coherence. Implementation. Scalability of Directory Coherence.

III. Assessment

Current control of knowledge is not provided.

An exam at the end of the course involves practical work for all students enrolled in the course. Topics covered by the test embraces all course material. If a student misses the exam because of some valid reason, s/he receives «absence» grade. The exam is assessed on usual 10-point scale.

IV. IV. Evaluation tools for student certification assessment

Current control of knowledge is not provided.

The knowledge gained in the course is evaluated on the exam.

The final control consists in passing an oral exam. The ticket contains 2 theoretical questions on the course of lectures. When answering the exam questions, the student must demonstrate knowledge of the subject area and sections studied within the discipline, clarity and literacy of the presentation of the material, give examples.

V. Reading list

5.1 Required

1. Tanenbaum, EH. Arhitektura komp'yutera. SPb. Piter, 2014. – 811 s. (Normativ obespechennosti studentov – 60 %).

2. Tanenbaum, EH. Arhitektura komp'yutera. SPb. Piter, 2011. – 843 s.(Normativ obespechennosti studentov – 40 %).

3. Materialy so stranicy izuchaemoj discipliny na sajte LMS (Normativ obespechennosti studentov – 100 %)

4. Obrazovatel'naya programma NIU VSHEH po napravleniyu 09.04.01 «Informatika i vychislitel'naya tekhnika» podgotovki magistra,magisterskaya programma«Komp'yuternye sistemy i seti» (Normativ obespechennosti studentov – 100 %)

a) Bazovyj uchebnyj plan NIU VSHEH Moskovskogo instituta ehlektroniki i matematiki po napravleniyu 09.04.01. "Informatika i vychislitel'naya tekhnika" podgotovki magistra (magisterskaya programma «Komp'yuternye sistemy i seti»), utverzhdennyj 6 maya 2016g.https://www.hse.ru/ma/system/learn_plans/

b) Rabochij uchebnyj plan NIU VSHEH NIU VSHEH Moskovskogo instituta ehlektroniki i matematiki po napravleniyu 09.04.01. "Informatika i vychislitel'naya tekhnika" Nacional'nyj issledovatel'skij universitet «Vysshaya shkola ehkonomiki» Programma discipliny «Vychislitel'nye sistemy»Oshibka! EHlement avtoteksta ne opredelen. Dlya napravleniya 09.04.01"Informatika i vychislitel'naya tekhnika" podgotovki magistra (magisterskaya programma «Komp'yuternye sistemy i seti»), utverzhdennym 6 maya 2016g. https://www.hse.ru/ma/system/learn_plans/

c) Programma discipliny «Vychislitel'nye sistemy» dlya napravleniya 230100.68 «Informatika i vychislitel'naya tekhnika» podgotovki magistra (magisterskaya programma/specializaciya «Informacionnye sistemy i komp'yuternye seti» i magisterskaya programma/specializaciya «Komp'yuternoe modelirovanie v tekhnike i tekhnologiyah») (2016/2017 uch. god). Lichnaya stranica Ivanovoj E.M. na sajte VSHEH http://www.hse.ru/org/persons/47633465

5. Federal'nyj Gosudarstvennyj obrazovatel'nyj standart vysshego obrazovaniya po napravleniyu podgotovki 09.04.01 Informatika i vychislitel'naya tekhnika (uroven' magistratury)ot

30 oktyabrya 2014 g. N 1420. http://www.hse.ru/ma/system/documents (Normativ obespechennosti studentov – 100 %)

6. Spravochnik uchebnogo processa NIU VSHEHhttps://www.hse.ru/studyspravka/

7. Organizacionno-pravovye dokumenty i lokal'nye akty/Polozhenie ob organizacii kontrolya znanij na sajte NIU VSHEH/razdel Dokumenty (http://www.hse.ru/docs/35010753.html).

8. Internet-resurs. MaterialyssajtafirmyIntel: Intel 64 andIA-32 ArchitecturesSoftwareDeveloper’sManual.http://www.intel.ie/content/dam/www/public/us

/en/documents/manuals/64-ia-32-architectures-software-developer-manual-325462.pdf(Normativ obespechennosti studentov – 100%

5.2 Optional

9. http://www.asciitable.com/

10. http://unicode-table.com/ru

11. IEEE Standard for Floating-Point Arithmetic http://ali.ayad.free.fr/IEEE_2008.pdf

12. Online Binary-Decimal Converterhttp://www.binaryconvert.com/index.html

13.Brojdo, V. L. Vychislitel'nye sistemy, seti i telekommunikacii. SPb. Piter, 2008.

14. A.P. Pyatibratov, L.P. Gudyno, A.A. Kirichenko. Vychislitel'nye sistemy, seti i telekommunikacii. Uchebnik. 2-e izd., pererab. i dop. Pod red. A.P. Pyatibratova. – M.: Finansy I statistika, 2004.

15.Top500 – cpisok 500 samyh bystryh v mire (http://www.top500.org/).

16. Materialy s sajta «Komp'yuter i ne tol'ko...», http://www.electrosad.ru/

17. Specializirovannyj rossijskij informacionno-analiticheskij novostnoj sajt iz sfery IT http://www.ixbt.com

18. Nezavisimoe rossijskoe onlajn-izdanie, posvyashchennoe cifrovym tekhnologiyam 3DNews DailyDigitalDigestwww.3dnews.ru

19. SajtkompaniiTezzaron/razdel 3T-iRAM technology http://www.tezzaron.com/technology/3TiRAM.htm

20. Veb-sajt Internet-izdaniya «Komp'yuterPress»http://compress.ru/

21. Biblioteka GOSTov i normativnyh dokumentov http://libgost.ru/

22. Maksimov N.V. Arhitektura EHVM i vychislitel'nyh sistem. Uchebnik — M.: YUNITI, 2005.

23.Materialy s sajta SD Company,/Stat'i/Komp'yuternaya tekhnika/Operativnaya pamyat'.(http://sd-company.su/article/computers/operativnaya-pamyat)

24. Testy proizvoditel'nosti processora. http://www.parallel.ru/computers/benchmarks/perf.html

25. NASParallel Benchmarks. http://www.nas.nasa.gov/publications/npb.html)

26. Sajt CSA(Computational Science Alliance)/razäeë Sravnitel'nayaproizvoditel'nost'. http://www.csa.ru/CSA/performance1.shtmr

27. CHernyak L. Flopsy i loshadinye sily // Otkrytye sistemy.2011. № 07. http://www.osp.ru/os/2011/07/13010474/

28. Sajt korporacii SPEC. http://www.spec.org/ Nacional'nyj issledovatel'skij universitet «Vysshaya shkola ehkonomiki» Programma discipliny «Vychislitel'nye sistemy»Oshibka!

EHlement avtoteksta ne opredelen. Dlya napravleniya 09.04.01"Informatika i vychislitel'naya tekhnika" podgotovki magistra
29. Bailey D. H. Twelve Ways to Fool the Masses When GivingPerformance Results on Parallel Computers, Ref: SupercomputingReview. Aug. 1991. P. 54—55. URL: http://www.pdc.kth.se/training/twelve-ways.html. Per. narussk.: Dvenadcat'sposobovobmana,predstavlyayaproizvoditel'nost'parallel'nyhkomp'yuterov.URL: http://favoritstudio.com/novostu-vusokix-texnologiy/desyatsposobov-obmana-na-rezultatax-izmereniyaproizvoditelnosti-gpu.html
30. Ivanova E. M. Sravnitel'naya ocenka proizvoditel'nosti vychislitel'nyh sistem // Informacionnye tekhnologii. 2013. № 8. S. 22-26.
31. Materialy s sajta http://ru.wikipedia.org
32. Materialy s sajta universal'nyj spravochnik-ehnciklopediya «ALL-IN-ONE» http://www.sci.aha.ru/ALL/b3.htm
33. Materialy sajta PC Magazinehttp://www.pcmag.ru/issues
34. A.V. Kalachev. Kurs lekcij Mnogoyadernye processory, Internet universitet – (http://www.intuit.ru/studies/courses/622/478/lecture/10859
35. Strukturnaya organizaciya yadra processor 64/Intel_Nehalemhttp://upload.wikimedia.org/wikipedia/commons/6/64/Intel_Nehalem_arch .svg?u selang=ru
36. Materialy sajta http://z52107.narod.ru/02_inf/01/05.html
37. Georgij ZHuvikin, Nanotranzistory, "Komp'yuterra" №3 ot 25.01.2005| Razdel: Tema nomera, http://old.computerra.ru/2005/575/37383/http://www.moluch.ru/conf/tech/archive/6/1217
38.Kuz'mina E. K., Monahova V. A., Curkin A. P. Polimernye tranzistory // Tekhnicheskie nauki: tradicii i innovacii: materialy mezhdunar. nauch. konf. (g. CHelyabinsk, yanvar' 2012 g.). CHelyabinsk: Dva komsomol'ca, 2012, s.83-88. http://www.moluch.ru/conf/tech/archive/6/1217/
39. Materialy sajta http://elementy.ru/news/430624
40. Materialy sajta http://www.dailytechinfo.org/infotech/
41. Materialy sajta www.membrana.ru
42. Materialy sajta http://ko.com.ua
43. Sergej Pahomov, Kvantovyj komp'yuter, Komp'yuterPress/stat'I http://compress.ru/article.aspx?id=17653
44. Materialy sajta http://eslitak.livejournal.com/241109.html

45.SetLlojd. ProgrammiruyaVselennuyu: Kvantovyj komp'yuter i budushchee nauki. – M.: Al'pina non-fikshn, 2013

46. Materialy sajta THG (RussianTom'sHardwareGuide)/ Razdel «processory»/D-WaveOrion: pervyj kvantovyj komp'yuterhttp://www.thg.ru/cpu/d-wave_orion/index.html

47. EHnciklopediya fiziki i tekhniki / stat'ya Dzhozefsonaehffekt http://femto.com.ua/articles/part_1/0991.html

48. Materialy sajta EE Times /KATALOG KOMPONENTOV / NOVOSTI EHLEKTRONIKI / Maks Maksfil'dhttp://datasheet.su/news/2514:2013-10-30

49. Materialy sajta http://www.nvidia.ru/content/PDF/kepler/NVIDIA-Kepler-GK110-Architecture-Whitepaper.pdf

50. Neupane, Mahesh (April 16, 2004). "Cache Coherence"

51. Azarov V. N., Vishnekov A. V., Leohin YU. L., Olejnik A. V., Ivanova E. M. Integrirovannye informacionnye sistemy obespecheniya kachestva i zashchity informacii / Nauch. red.: V. N. Azarov. M. : MIEHM, 2003.

52. Sajt ttps://nvworld.ru/ razdel «articles» stat'ya «Parallel'nye vychisleniya na GPU NVIDIA ili superkomp'yuter v kazhdom dome» URL: https://nvworld.ru/articles/cuda-parralel-for-home/

53. Kurs lekcij po CUDA na VMK MGU http://www.nvidia.ru/object/cuda_state_university_courses_new_ru.html

54.Obzor i test chetyrekh modulej operativnoj pamyati DDR3. https://www.overclockers.ru/lab/62500_4/Obzor_i_test_chetyreh_modulej_operativnoj_pamyati_D DR3-1600_Crucial_Ballistix_Sport_VL_LOW_Profile_obemom_8_Gbajt.html Nacional'nyj issledovatel'skij universitet «Vysshaya shkola ehkonomiki» Programma discipliny «Vychislitel'nye sistemy»Oshibka! EHlement avtoteksta ne opredelen. Dlya napravleniya 09.04.01"Informatika i vychislitel'naya tekhnika" podgotovki magistra https://www.overclockers.ru/lab/62500_4/Obzor_i_test_chetyreh_modulej_operativnoj_pamyati_DDR 3-1600_Crucial_Ballistix_Sport_VL_LOW_Profile_obemom_8_Gbajt.html

5.3 Software

№ п/п	Title	Access conditions
1.	Browser	*From the university's internal network (contract)*

5.2 Professional databases, information reference systems, Internet resources (electronic educational resources)

№ п/п	Title	Access conditions
	Professional databases, information reference systems	
1.	Consultant Plus	*From the university's internal network (contract)*
2.	Electronic library system Urayt	URL: https://biblio-online.ru/
	Internet resources (electronic educational resources)	
1.	Open education	URL: https://openedu.ru/
2.	Electronic encyclopedia of processor terms.	http://www.ixbt.com/cpu/cpupedia.shtml

5.3 Material and technical support of the discipline

Computer classroom with Internet.