КИМ по курсу «Computer Architecture»

1. Architecture and Microarchitecture. Machine Models.
2. [Microcoded Microarchitecture](https://www.coursera.org/lecture/comparch/microcoded-microarchitecture-2yOX6). Pipeline Basics. Structural Hazard. Data Hazards.
3. [Control Hazards, Jumps](https://www.coursera.org/lecture/comparch/control-hazards-jumps-ApN1O). Control Hazards, Branch. Control Hazards, Others. Memory Technologies.
4. Classifying Caches. Cache Performance. Superscalar. Basic Two-way In-order Superscalar. Fetch Logic and Alignment.
5. Baseline Superscalar and Alignment. Interrupts and Bypassing. Interrupts and Exceptions. Introduction to Out-of-Order Processors.
6. Review of Out-of-Order Processors. I2O2 Processors. I2O1 Processors. IO3 Processors. IO2I Processors.
7. Register Renaming Introduction. Register Renaming with Pointers to IQ and ROB. Register Renaming with Values in IQ and ROB. Memory Disambiguation.
8. Limits of Out-of-Order Design Complexity. Introduction to VLIW. VLIW Compiler. Optimizations. Classic VLIW Challenges. Introduction to Predication.
9. Scheduling Model Review. Review of Predication. Predication Implementation. Speculation Execution. Dynamic Events and Clustered VLIWs. Case Study: IA-64/Itanium.
10. Branch Prediction Introduction. Static Outcome Prediction. Dynamic Outcome Prediction. Target Address Prediction.
11. Basic Cache Optimizations. Cache Pipelining. Write Buffers. Multilevel Caches. Victim Caches. Prefetching.
12. Multiporting and Banking. Software Memory Optimizations. Non-blocking Caches. Critical Word First and Early Restart.
13. Memory Management Introduction. Base and Bound Registers. Page Based Memory Systems. Translation and Protection. TLB Processing.
14. Address Translation Review. Cache and Memory Protection Interaction. Vector Processor Introduction. Vector Parallelism. Vector Hardware Optimizations. Vector Software and Compiler Optimizations.
15. Reduction, Scatter/Gather, and the Cray. SIMD. GPUs. Multithreading Motivation. Coarse-Grain Multithreading. Simultaneous Multithreading.
16. SMT Implementation. Introduction to Parallelism. Sequential Consistency. Introduction to Locks.
17. Sequential Consistency Review. Locks and Semaphores. Atomic Operations. Memory Fences. Dekker's Algorithm.
18. Locking Review. Bus Implementation. Cache Coherence. Bus-Based Multiprocessors. Cache Coherence Protocols.
19. More Cache Coherence Protocols. Introduction to Interconnection Networks. Message Passing. Interconnect Design.
20. Networking Review. Topology. Topology Parameters. Network Performance. Routing and Flow Control.
21. Credit Based Flow Control. Deadlock. False Sharing. Introduction to Directory Coherence. Implementation. Scalability of Directory Coherence.